Pixel detectors for linear collider

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- Monolithic Pixel Detectors
- 3D pixel detectors
- Hybrid Pixel Detectors
- Raditaion Hardness

Physics benefits of better vertex resolution (apart from the obvious improvement in $\sigma_{\Delta z}$)

- Combinatorics
  - Inclusive (e.g. $K^{*0} \to K^- \pi^+$) ♠
  - $B \to D^0 D^-, D^+ D^-, D^0 K^-$ etc. ♠

- Charm vertex $\to$ tag-side z resolution. ♠

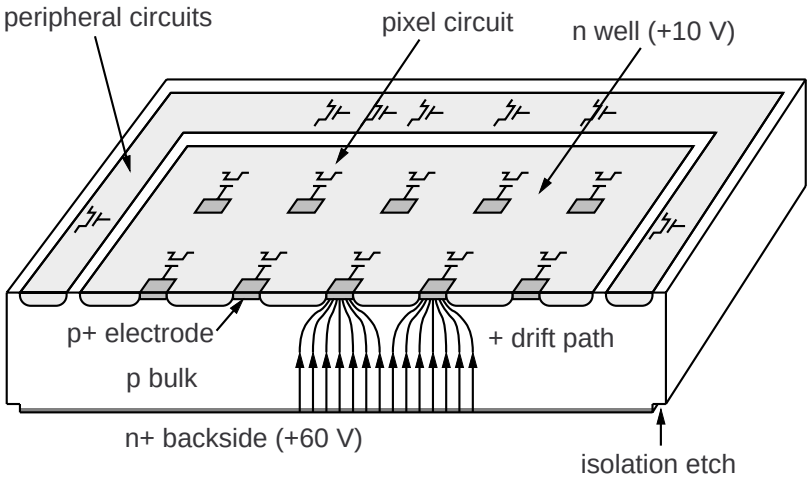
- Vertical B travel: $\to \Delta z \to \Delta t$

  Currently, the correction makes the resolution worse (crude calculation). ♠

- Continuum suppression by Δz ♠

Monolithic Pixel Detector

Readout electronics and sensor on the same chip



Hawaii-Stanford monolithic pixel detectors
Fabricated at CIS, Stanford

- Thickness 300μm

- Collection electrode: p^+ (i.e. collects holes)
- Bulk: p
- Backside: n^+-diffusion

- One PMOS readout circuit in n-well for each pixel.

- Operated with full depletion at $\sim$60 V.

Two versions of monolithic pixel detector succesfully tested:

V1. 1993. Pitch $34 \times 125 \mu m^2$
1.02mm×1.02mm active area
Full readout

Tested at Fermilab (muon beam)
$\rightarrow \sigma = 2.0 \mu m$ ($34 \mu m$ pitch direction)

V2. 1996. Pitch $65 \times 67 \mu m^2$
32×32 array ($\sim$ $1 mm^2$ active area)
Sparse readout
Tested by ^{241}Am

Monolithic Pixel Detector Test Setup.

^{241}Am 60keV γ
(MIP ~ 1000 keV)

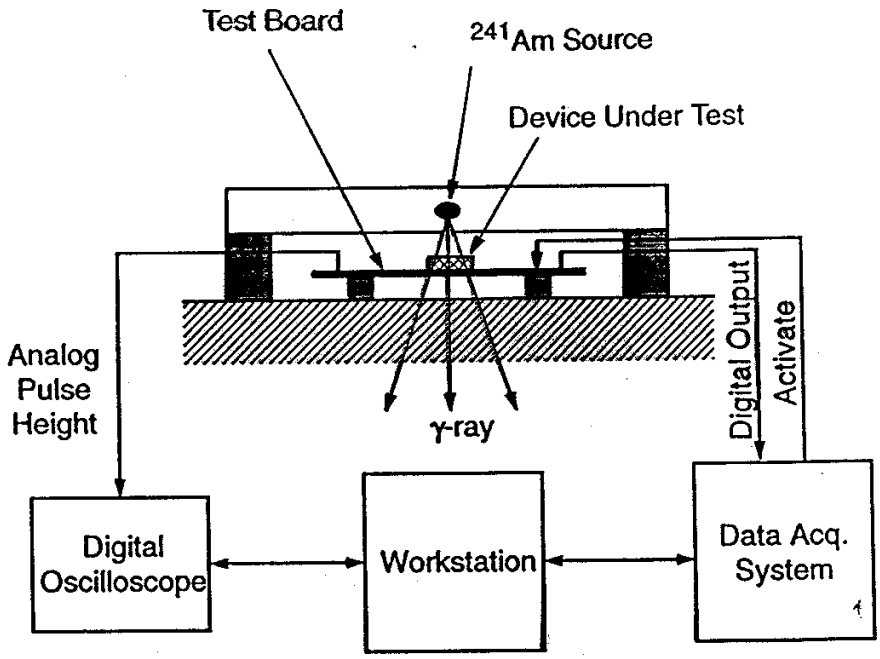
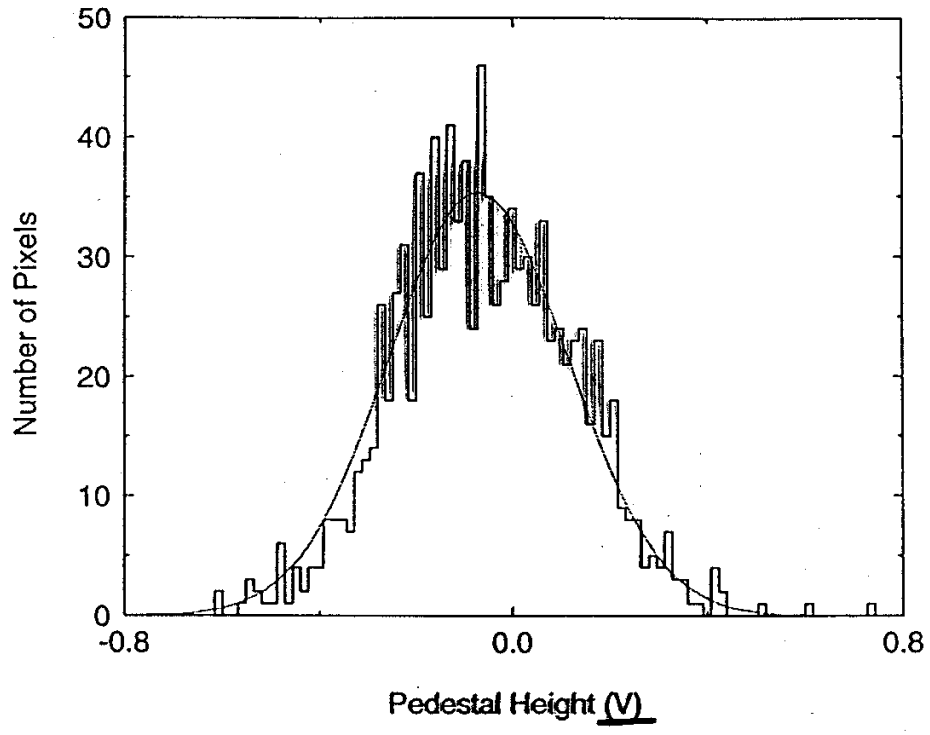
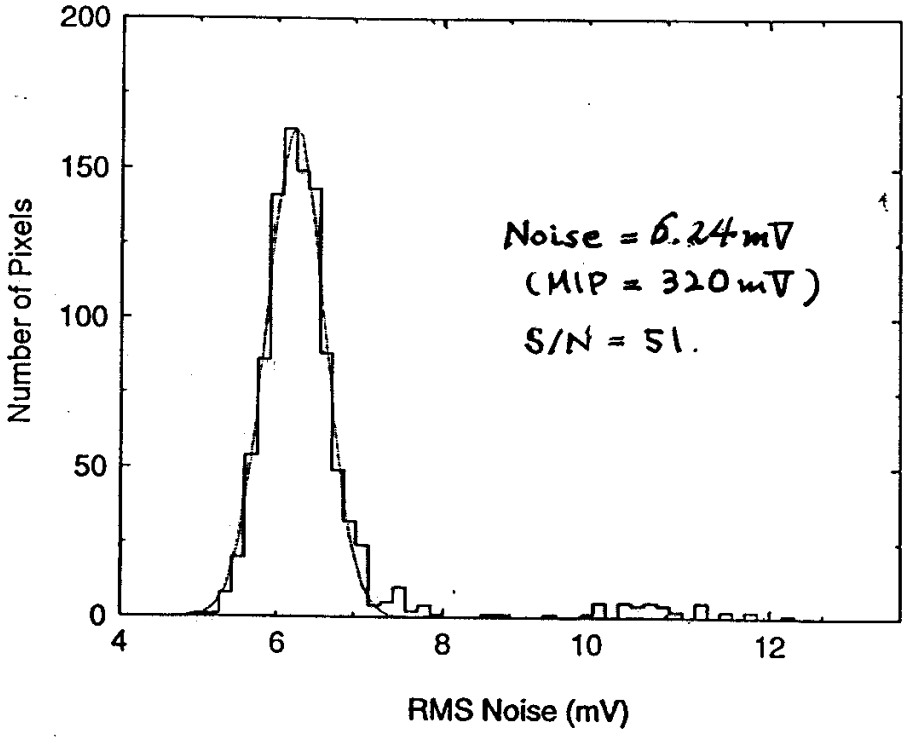
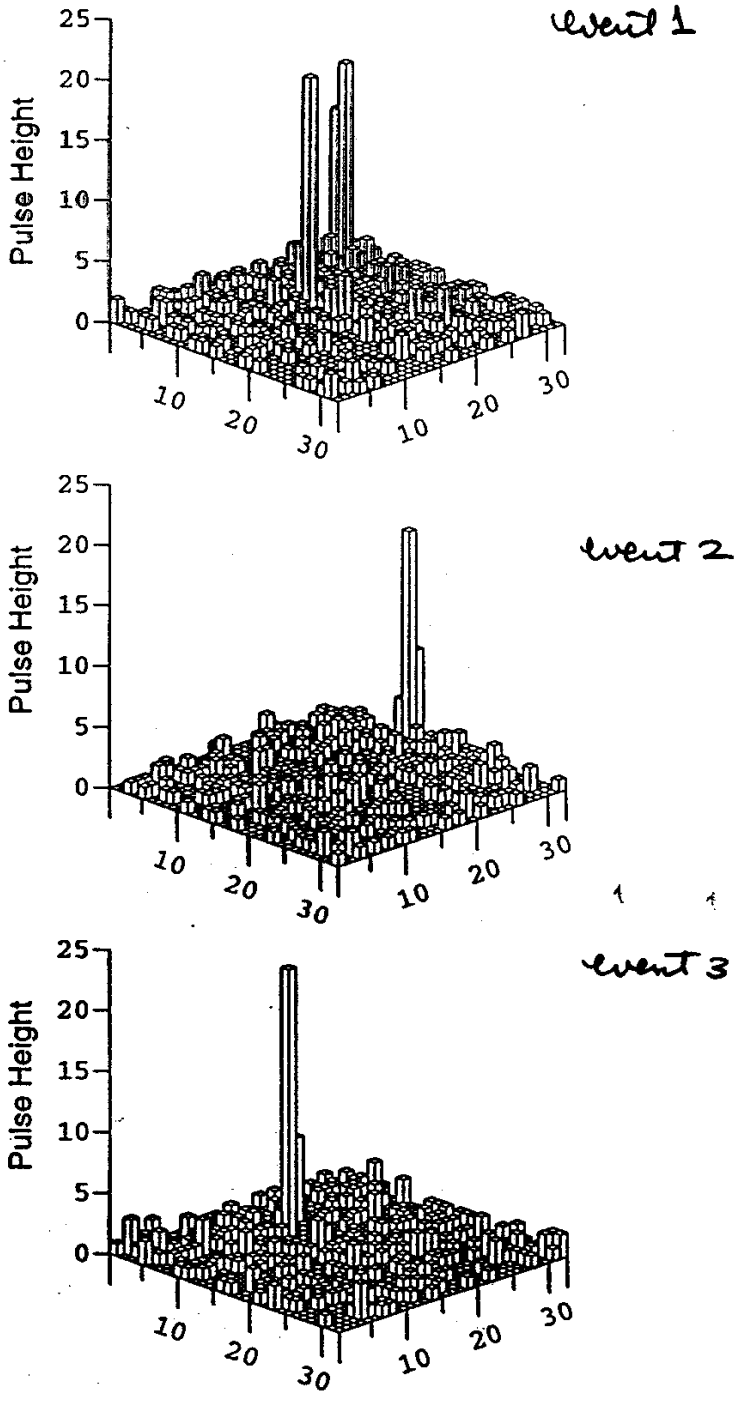


Figure 5.4: Block diagram of a typical γ-ray experimental set-up.


Number of Pixels
50
40
30
20
10
0
-0.8
0.0
0.8
Pedestal Height (V)


Number of Pixels
200
150
100
50
0
4
6
8
10
12
RMS Noise (mV)
Noise = 6.24mV
(MIP = 320mV)
S/N = 51.

241 Am Test.


event 1
Pulse Height
25
20
15
10
5
0
10
20
30
10
20
30
event 2
Pulse Height
25
20
15
10
5
0
10
20
30
10
20
30
event 3
Pulse Height
25
20
15
10
5
0
10
20
30
10
20
30

Challenges for the monolithic pixel design:

1. Larger array

Using the same sparse readout scheme, 320×320 array (1 cm^2), 0.5% pixel occupancy
$\rightarrow \sim 300\mu s$ readout.

But, at this size most of the rows are hit (the sparse readout operates on rows) $\rightarrow$ might as well read all rows (future)

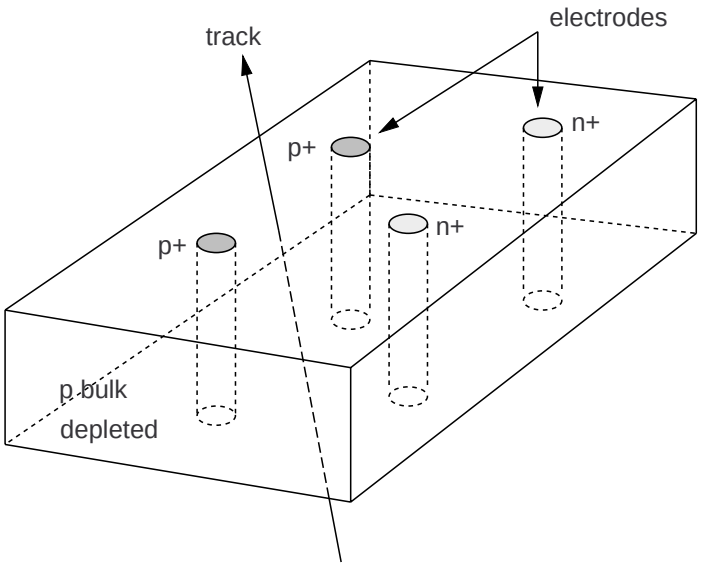
2. Foundry

Difficult to find a foundry who is

- willing to closely collaborate,
- has deep-submicron technology,
- can respond to non-standard facbrications: rad-hard design, high-purity bulk silicon.

$\rightarrow$ keep looking for a foundry,
but pursue hybrid design meanshile.

3D Pixel Detector



- Low depletion voltage - a few V or less
  $< 10V$ even after LHC-level radiation
  $\rightarrow$ 'rad-hard'
- Fast. Pulse width $\sim$ 1 ns
- Thickness and drift distance are decoupled
- Top potential = bottom potential
  $\rightarrow$ possibly active to the edge

Current status of 3D Pixel Detector

- Plasma etching can make precise vertical holes needed for 3D pixel.

- p/n junction verified
  (full depletion @5V for 100μ pictch)

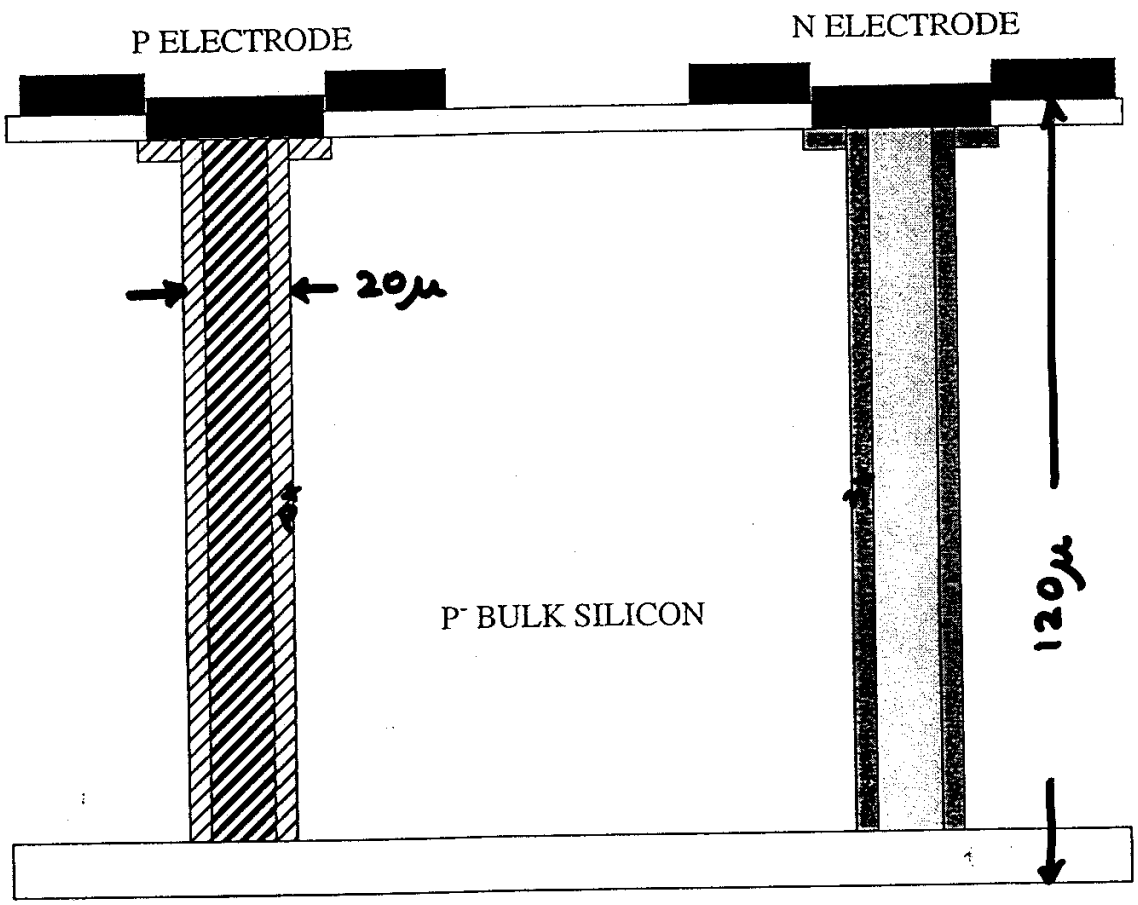
- IR pulse test succesful.

Plan

- Wire-bond to existing readout electronics
  perform β-ray test and radiation test.

- bump-bond to the ATLAS readout chip.

DEVICE CROSS SECTION



P-TYPE POLYSILICON

N-TYPE POLYSILICON

P-TYPE DIFFUSION

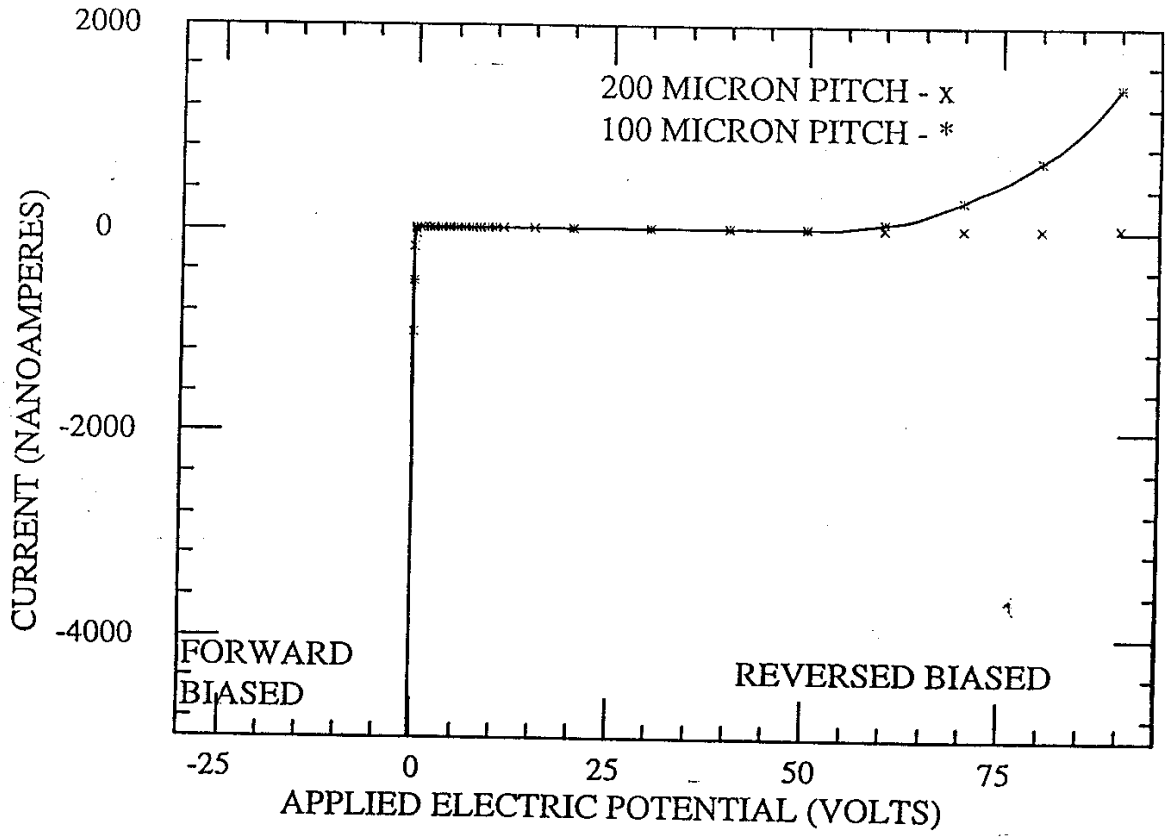
N-TYPE DIFFUSION

ALUMINUM

THERMAL OXIDE

3D Pixel (Hawaii - Stanford)

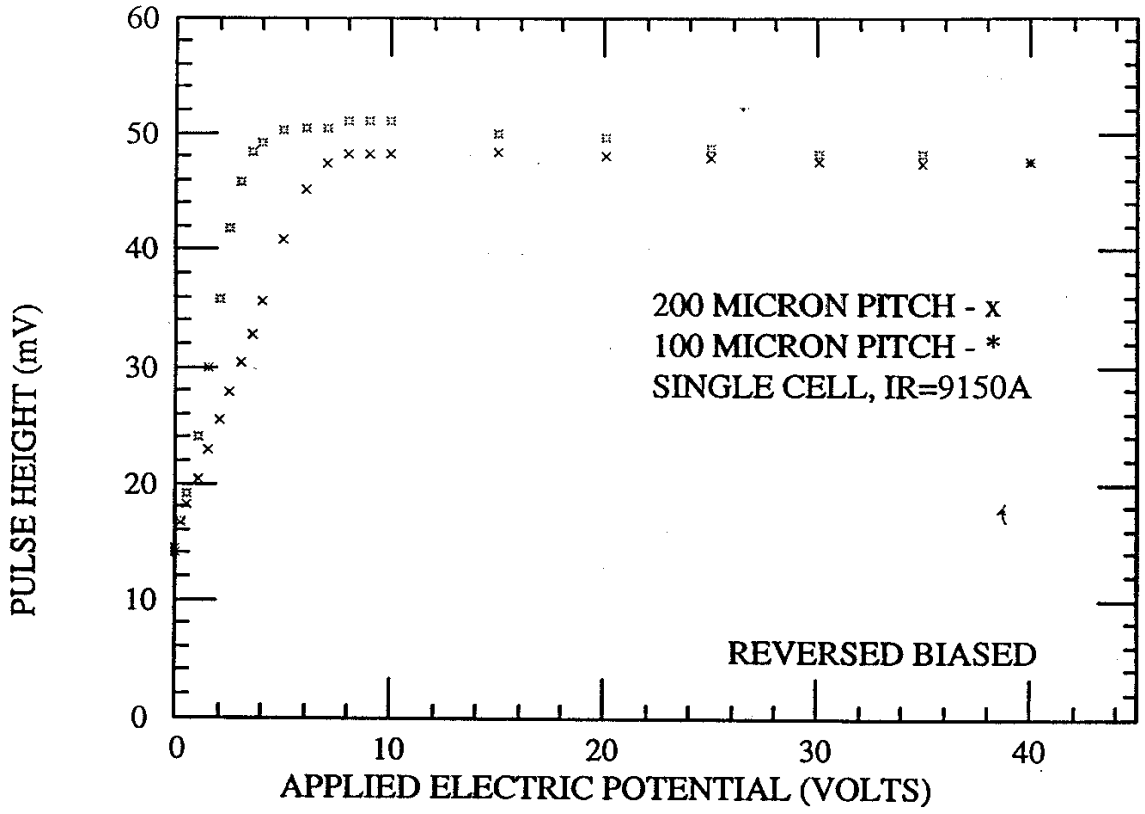
Test of P-N junction



3D Pixel

IR pulse test

- 100μ pitch : fully depleted @ ~5V

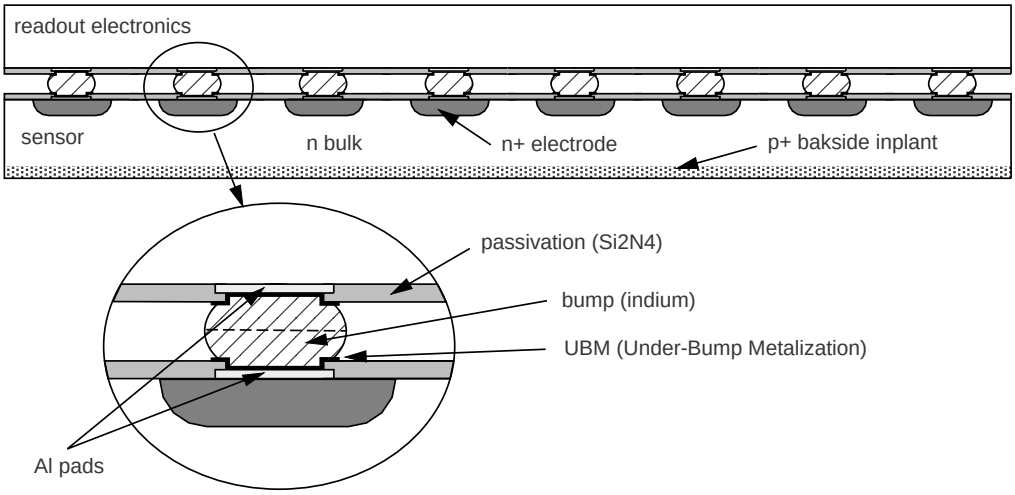


Hybrid Pixel Detectors

Hybrid = Bump-bonded

Sensor: high-resistivity silicon (typically float-zone)
Readout chip: Commercial CMOS OK

→ Fabricate separately and bond them
(flip-chip technology)



Most current and proposed HEP pixel detectors uses hybrid design.
(DELPHI, WA97, ATLAS, CMS., ALICE, BTeV...)

	pixel size	# pixel (total)	sensor thickness	heat/cell
DELPHI	$330\times330\mu^2$	1.2 M	300μ	40μW
WA97	$50\times500\mu^2$ $75\times500\mu^2$	1.2 M	300μ	
ATLAS	$50\times300\mu^2$	105 M	200-250μ	50μW
CMS	$150\times150\mu^2$	56 M	200-250μ	60μW
ALICE	$50\times300\mu^2$	15.7 M	150μ	30μW
BTeV	$50\times300\mu^2$	60 M	300μ	$<40\mu$W

Issues for a LC detector:

(a) Readout electronics (that fits in $35\times35\mu^2$)

(b) Thinning of sensor and readout chips

(c) Bump bonding

(d) Radiation hardening

(a) Proposed readout electronics

(Conceptual design by G. Varner)

- Avoid sending analog signal by digitizing on each pixel.
- V_{ramp}+Comparator and 5-line counting bus. LVDS driver at the end of sensor.
- 1cm$\times$3cm, $50 \times 50 \mu\text{m}^2$ pixel. 2% occupancy $\rightarrow$ 200μs read out time.

Expected heat generation

- Most of the time the MOS transistors do not dissipate heat, namely static.
  (much easier situation than LHC)

- Needs a completed design of the circuit,
  but roughly, $\sim$0.4μW/pixel
  $\rightarrow \Delta T \sim 0.1$°K (side cooing)

- LVDS driver generates lots of heat, but it is at the end of sensor.

(b) Thinning of the sensor and readout chip

- Wafer thinning is a routine commercial process (for heat dissipation)

  $$\begin{cases} \text{Grinding-polishing-etching} \\ \text{Plasma etching} \end{cases}$$

- Readout electronics:
  Thinned after fabrication using a commercial process (e.g. MOSIS).

- Sensors may be thinned first.
  (needs a dedicated foundry)

  Or, thinned after fabrication
  (still needs some processing of the thinned side)

- Thin before or after the bump bonding?

  If thinned after bonding, the read-out electronics may be made quite thin ($\sim 20\mu$?).

  $\rightarrow$ **more R& D needed.**

(c) Bump bonding

- Bump bonding defects $< 10^{-4}$ (dummy tests).

But some problems reported for the real ATLAS detector.

- Bump diameter can be $< 10\mu$,
  pitch can be $< 20\mu$
  (e.g. GEC Marconi)

Two types of bumps

	Indium	Solder
UBM *	simple	complicated
bump deposition	both sides	one side
connection	pressure	fused
Strength (4K bumps) (tension& sheer)	2.5 lb	10-14 lb (strong)
alignment required	1-2μ	$\sim 10\mu$ (self-sligning)
resistance/bump	1-2 Ω (poor)	2-3 $\mu\Omega$ (good)

* UBM = Under Bump Metalization

(d) Radiation Hardening

Radition damage effects
- a) Effective dopant creation
- b) Leakage current increase
- c) Threshold shift of MOS transistors

a) Effective dopant creation

Mostly p type

- Change in $V_{\text{depletion}}$ (e.g. increase)
  $\rightarrow$ high voltage breakdown, partial depletion
- Type conversion ($n \rightarrow p$) at high dose
  (OK for Belle)

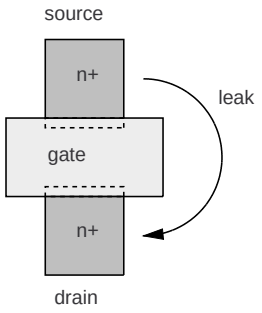
$\rightarrow$ Design the detector such that it can stand high voltage
(e.g. guard rings at the edges of sensor)

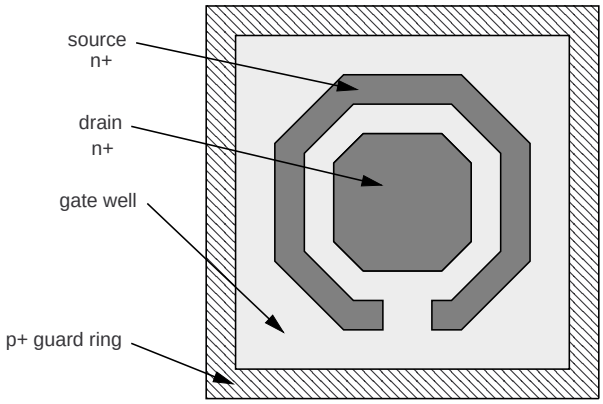
b) Leakage current

1. source-drain leakage
2. inter-transistor leakage
3. detector bulk leakage current

Strategy:

- Rad-hard design rules
  - Surround-gate design
  - p-stop around NMOS transistor

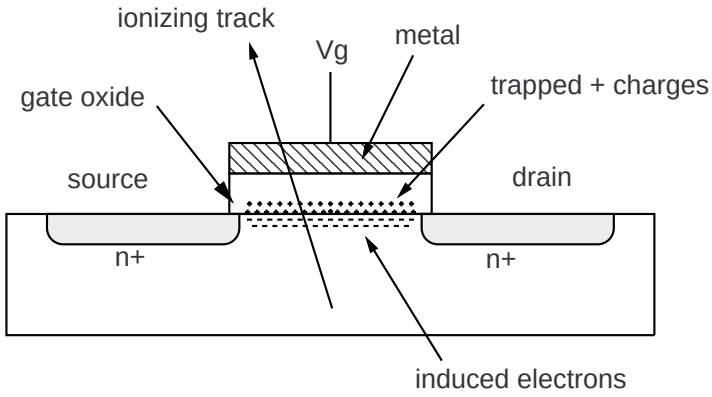




- current compensation for detector leakage (read-out electronics design)

c) Threshold shift of MOS transistor

Trapped positive ionization charges at gate-oxide
$\rightarrow$ induces elctrons just below the gate.



$$\Delta V_{\text{th}} \propto \begin{cases} t^2 \ (t < 10\,\text{nm}) \\ t^3 \ (t < 10\,\text{nm}) \end{cases}$$

t: gate thickness

Make the gate oxide thin:
$\leftarrow$ natural result of small scale processes.
(e.g. commercial IBM $0.25\,\mu$ process)

Pixel detector status summary:

1. Monolithic pixel proven to work (32×32 array).

   Challenges:
   - larger detector
   - rad-hardness
   - **foundry !!**

   → try hybrid design.

2. Hybrid pixel design

   - heat $< 50\mu$W/pixel for LHC.
     Less for Belle → probably not a problem.
   - thickness $< 250\mu$ (sensor & read-out)
     being tested. 150μ total seems feasible.
   - bump bonding

     yield $> 99.99\%$:dummy test
     (some problems with real detectors)

     pad size can be $< 10\mu$, pitch can be $< 20\mu$
   - Rad-hardness of readout chip
     Deep subμ + rad.hard rules →
     30 MRad : IBM 0.25μ (ALICE)
     (Barely fits in $50 \times 300\mu^2$)

R& D Items Summary:

1. Readout electronics that fits in pixel and rad-hard.

2. Thinning of sensor ($\sim 100\mu$)
   and readout chip ($\sim 50\mu$).

3. Bump bonding for our specifics.

On-going efforts:

Prototype design

2mm$\times$2mm
pixel: $50\mu \times 100\mu$

- Readout electronics design by G. Varner.
  MOSIS submission in a few months.

- Sensor design by S. Parker and C. Kenney.
  To be fabricated at CIS in the same time scale.

- Bump-bonding test: in contact with GEC Marconi.
  Other companies are to be tested.