

TRIGGER & DAQ

Convenors : Il Hung Park & Patrick Le Du

- The next 10 years of trigger/DAQ P. Le Du (Saclay) 15 min
- Performance of switching networks J.P. Dufey (CERN) 40 + 5 min
- JLC Trigger and DAQ Dr Ueda (~~KEK~~^{TOKYO}) 25 + 5 min
- BREAK
- NLC Trigger and DAQ (J.J. Raaijse) 25 + 5 min
- TESLA "Software Trigger" R.Gerhards (DESY) 25 + 5 min
- Discussion organized as a "round table" ...
Detectors Electronics constraints
Trigger strategies issues
"on and off line" boundaries....

larger-scale production

1989 → 1999 → 2009

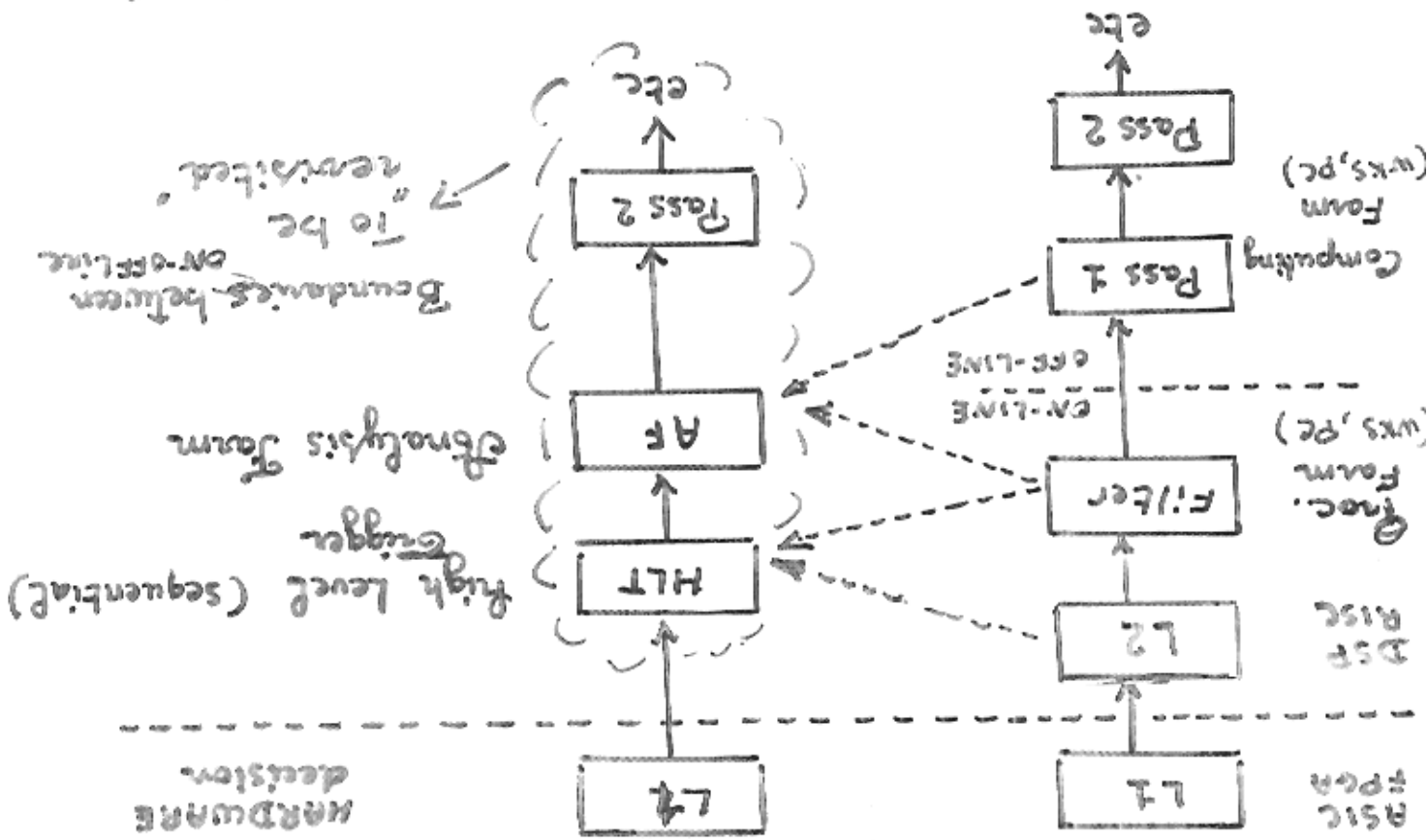
- Increasing use of "commodity" components
- Take advantage of "industry standards"
- Technology "forecast" : → very favorable.

	DRAM	Proc. Power
LEP-1989	128-512 KB	1-5 Mips
Today 1999	4-8 MB	≈ 400 Mips
2004 - 2009	> 64 MB	≥ 5 Gips

(x100)
(x10-100?)

➤ Memory and Processing Power quasi "unlimited"

• Flexible Boundaries for Processing Strategies:



➤ more complex algorithms are moving "on-line"

➤ on-line and off-line boundaries are flexible

New concept of the "computing model"

T-DAQ

J.J. Ruszel SIAC
(on behalf)
by email 26/04/99

NLD Thoughts

(an update of the keystone meeting)

• 2 remarks:

Both → Simple : in T/DAQ nothing technologically challenging.

→ Complex : running linear Collider is unlike running any other type of accelerator.

➤ High Quality Beam on every Bunch very challenging.

➤ More intimate connection between Machine and Detector
ex: SID → very limited subset of detector available
on every Bx.

2/3

• TI/OAD = Some radical approach:

→ Moving everything (all "policy") out of the embedded systems part of the OAD. (selection algorithms ...)

➤ {No Real Time Trigger}

→ Avoid OAD to be vertically integrated (like BBan!)

... political and logistic nightmare

➤ Clear separation of boundaries.
definition

→ Is it technically feasible?

➤ OAD detector elements must run in a un-triggered mode.
what about VTX?

➤ Packaging and shipping data to generic General Purpose processors.

➤ Route "bad pulses" to accelerator people.

➤ Replace "feature extraction" Algorithms by Semi-Post data compression

Some ideas ... to be explored!

• on Technologies:

- try to take advantage of what the future brings.
- High Bandwidth, but not very Low Latency. networks
 - Busses will be less important and perhaps non-existent (ex: machine is moving on no. buses for reliability reasons!).

Storage

DST

Files 4:10

Row data

per B train
Total = 340M

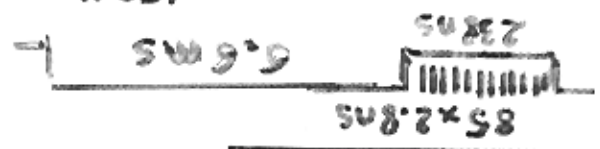
- $\mu = ?$
- CAT: 21M \rightarrow 32 KB
- CDC: 47M \rightarrow 42 MB
- VTX: 320M \rightarrow 1.4 MB

Data Volume

- no hardware trigger logic
- DR triggered every train Xing
- Bunch ID by "off line"

Concept: —

x 150 Hz



Bunch Structure

107 Bytes/day (eg. LHC)

100 MB/sec

1.6 GB/s

16 GB/s

13.5 MB

→ ? ←

S

40 MB/s

13 GB/s

33.5 MB

400-800M

- CCD = 840M
- APS = 400M
- TPC = 720K
- FWSI = 10M
- calor = 340K
- muons = 200K

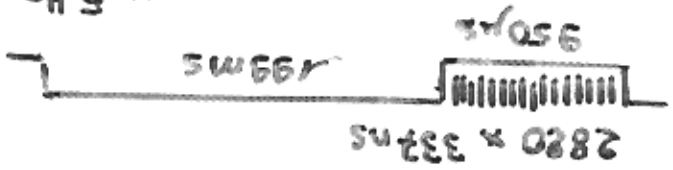
- Sw selection between trains

- Zero suppression or/and data compression ...

- No hardware trigger

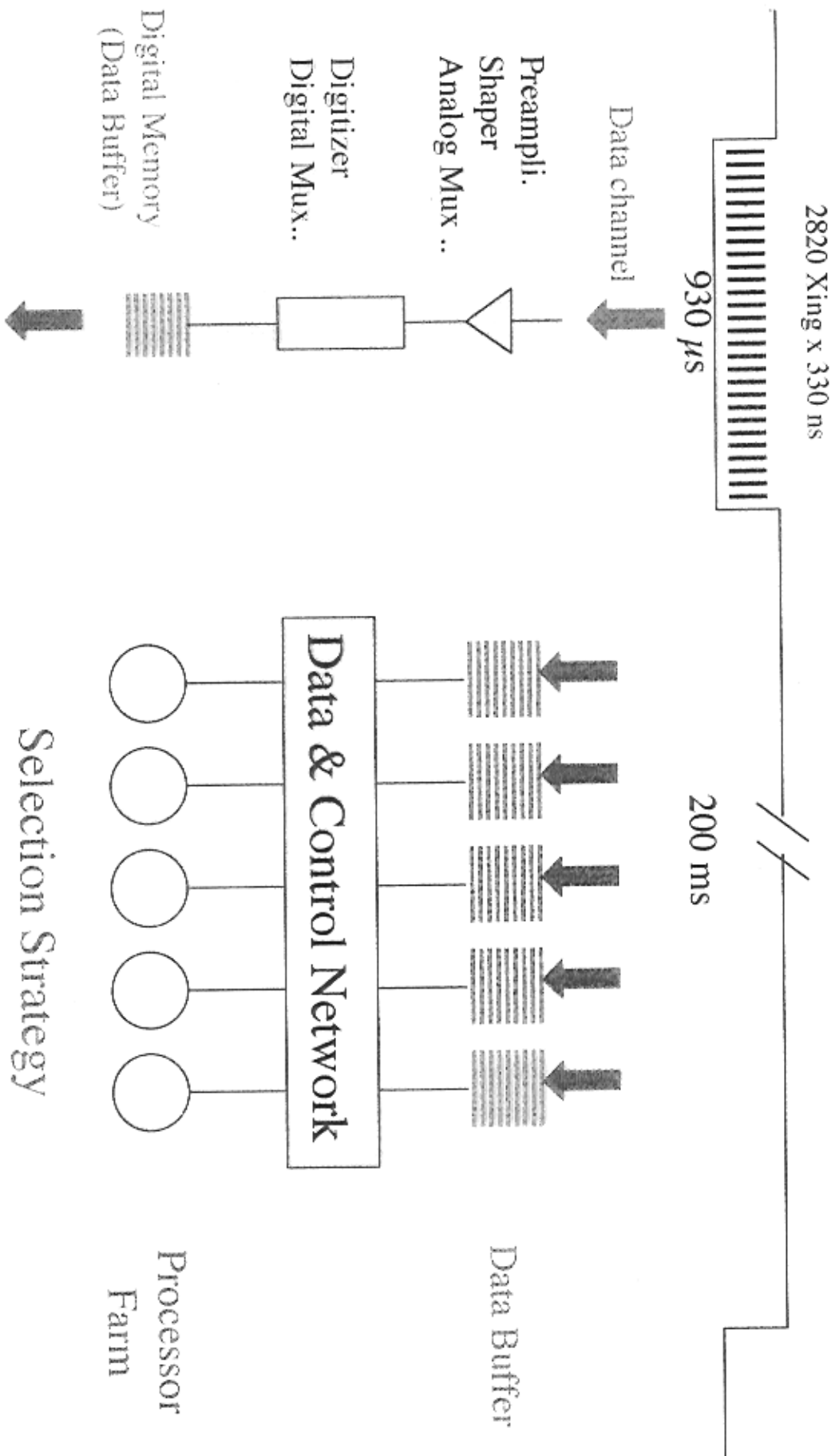
- Store data of one Bunch train

x 5 Hz



(in parallel)

Tesla "Software Trigger" concept



- Build & format event
- Classify & store "bunches"
- Select & analyze "Bunch Of Interest" ...

Conclusion

- No hardware trigger
 - dead time free
 - no compromise on physics } No data loss
 - flexible (programmable ...)
 - cost effective (OTS technologies)
 - scalable
 - portable (off-line sw in on-line env.)
- Nothing technologically challenging.
- Constraints on "Front End Electronics"
 - CCD, TPC
 - Bunch ID (NIC/JIC)
 - Read 1ms continuously (Tesla) ↗ (Occupancy)
- "On-offline" computing model (Common)
 - event selection/rejection strategies
 - event analysis and processing. (common resources ...)
 - event reads ... event/data compression!