ATF cavity BPM system
April 27, 2005

Overall: System is designed to measure 25 cavity BPMs (X and Y) for the ATF2 project.

Performance: System noise performance is estimated to be approximately 2dB worse than the existing SLAC electronics. If the existing system is electronic noise limited, this would correspond to a resolution of approximately 30nm. The system linearity is approximately 6dB lower than for the existing SLAC cavity bpms. For similar processing algorithms, this would imply ½ the dynamic range of the SLAC system (assuming gain set for 30nm resolution).

Note that the calculated resolution is ~3nm, however resolution at this level has not been demonstrated in the SLAC system.

The system dynamic range is expected to be approximately 500 microns, extendable by more complex processing algorithms (looking at the "tail" of the decay).

Design: The basic concept is similar to the SLAC processing electronics, however with several detail differences. Rather than use narrow band filters to reject out-of-band noise, "image reject" mixers are used. In this application where there are not strong interference signals, this provides good performance, with a much simpler system.

The system is constructed form surface mount components, resulting in a compact and low cost design.

Design details:

A calibration coupler is provided at the input of the electronics. This allows a tunable RF source to be reflected from the Cavity BPM to provide electronics calibration, and cavity frequency measurement.

The C-band front-end is conventional, with the system noise figure set by the pre-amplifier. The 4dB noise figure of this amplifier is acceptable, however work is underway to find a lower noise solution.

The image-reject mixer is a part from Hittite (HMC525LC4), with an external IF 90 degree hybrid. This will provide >20dB rejection of the unwanted sideband. The mixer performance (7.5dB loss, 24dB IP3) is similar to the mixers used on the SLAC electronics.

A series of amplifiers is used for the IF. A 1.7dB noise figure amplifier from Macom is used as a pre-amp. This is followed by a medium power, and then high power amplifier from MiniCircuits. System linearity is limited by the final output amplifier (a MiniCircuits HELA-10D) operated at low voltage to reduce power consumption.

Bandpass filters after the amplifiers are used to reject out-of-band noise. These filters (at 20MHz) are constructed from discrete components.

Anti-alias / noise rejection filters are mounted at the input of the digitizers.

Digitizer subsystem:

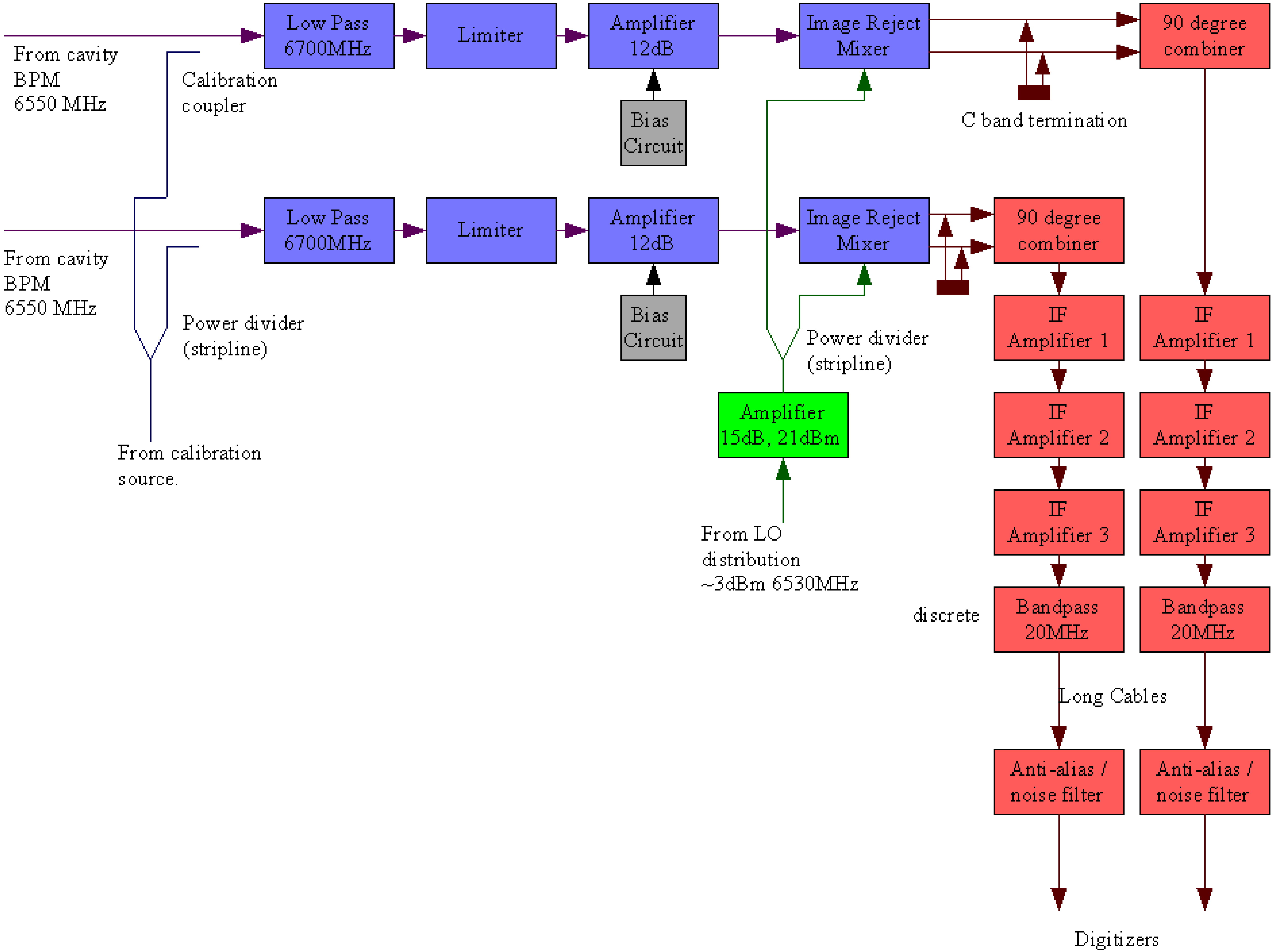
14 bit, 119MS/s digitizers from SIS (similar to the existing SLAC Nanobpm system) are used. The baseline design is for 3 cavities, a reference signal, and a beam time reference to be sent to each digitizer – requiring 9 digitizers for the system. This can be reduced to 7 digitizers if good clock – to – clock skew can be demonstrated.

LO and clock source:

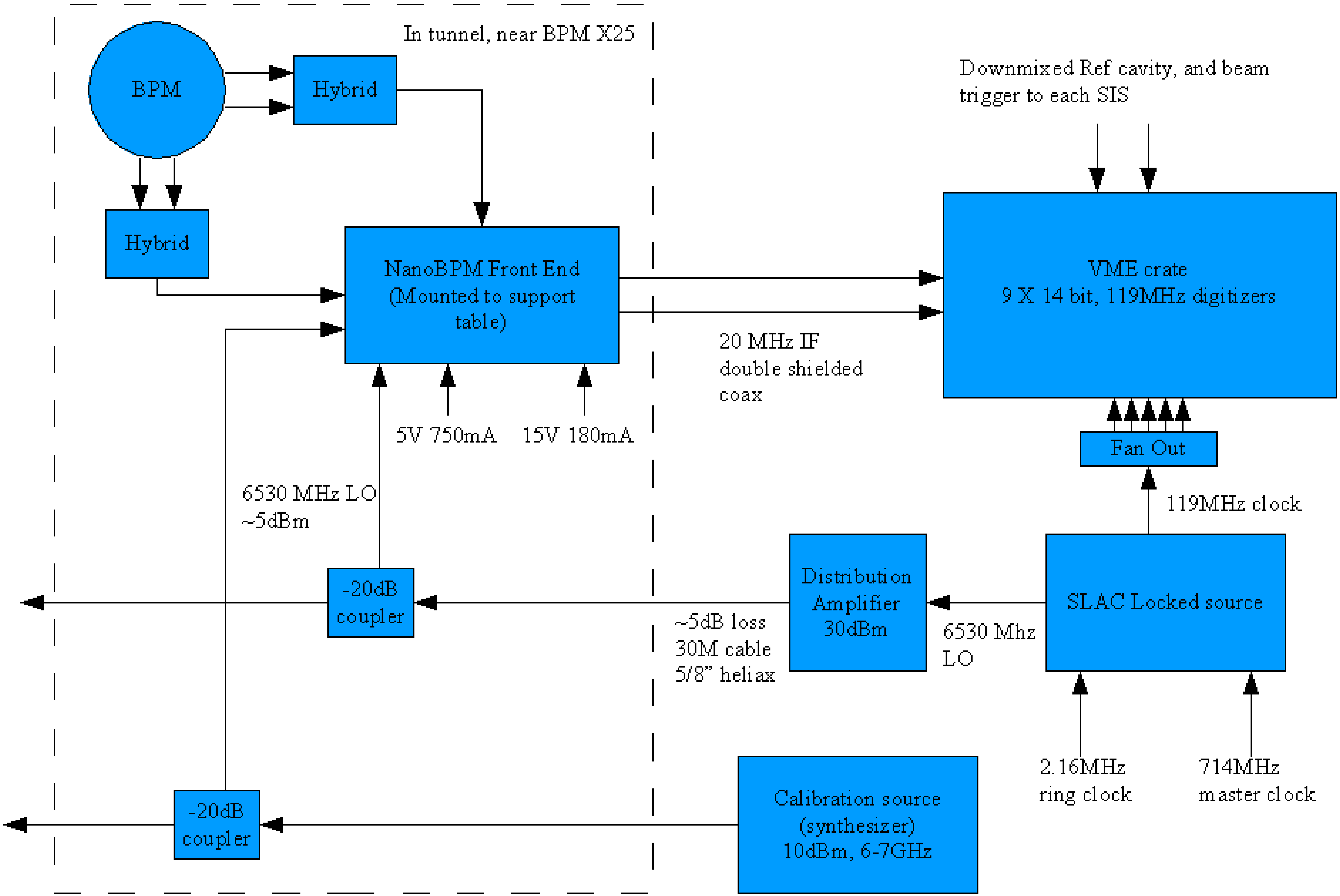
The LO and clock source being developed for the SLAC nanobpms can be modified to produce the frequencies required for the ATF2 system. It is assumed a spare unit will be produced.

Costs: Costs in the attached spreadsheet are "component" costs only. No R+D, spares, etc are included.

The cost is dominated by the digitizer system, estimated at $65,000. The RF boards cost is only $11,000 (due to the low cost construction). The remainder of the estimated $113,000 total system component cost is comprised of miscellaneous components – estimated in the attached spreadsheet.



From cavity BPM 6550 MHz
Calibration coupler
Low Pass 6700MHz
Limiter
Amplifier 12dB
Bias Circuit
Image Reject Mixer
90 degree combiner
C band termination
From cavity BPM 6550 MHz
Power divider (stripline)
From calibration source.
Low Pass 6700MHz
Limiter
Amplifier 12dB
Bias Circuit
Image Reject Mixer
90 degree combiner
Power divider (stripline)
Amplifier 15dB, 21dBm
From LO distribution ~3dBm 6530MHz
IF Amplifier 1
IF Amplifier 2
IF Amplifier 3
discrete
Bandpass 20MHz
IF Amplifier 1
IF Amplifier 2
IF Amplifier 3
Bandpass 20MHz
Long Cables
Anti-alias / noise filter
Anti-alias / noise filter
Digitizers


In tunnel, near BPM X25
BPM
Hybrid
Hybrid
NanoBPM Front End
(Mounted to support
table)
5V 750mA
15V 180mA
6530 MHz LO
~5dBm
-20dB
coupler
-20dB
coupler
Downmixed Ref cavity, and beam
trigger to each SIS
VME crate
9 X 14 bit, 119MHz digitizers
20 MHz IF
double shielded
coax
Fan Out
119MHz clock
Distribution
Amplifier
30dBm
SLAC Locked source
~5dB loss
30M cable
5/8" heliax
6530 Mhz
LO
2.16MHz
ring clock
714MHz
master clock
Calibration source
(synthesizer)
10dBm, 6-7GHz